INFORMATION DISCLOSURE CITATION FORM FOR PATENT APPLICATION (FORM PTO-1449) (Substitute)	Docket No.: 909A.0150.U1(US) Serial No.: 10/733,537 Applicant(s): Kim et al. Filing Date: 12/11/03 Group: 2819

U.S. PATENT DOCUMENTS

Examiner Initials	Document Number (Number-Kind Code)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant	Class	Sub-class
	US-				
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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS (Author (Capitalize), Title, Date, Pages, Etc., if known)

pl	"A Precise On-Chip Voltage Generator for a Gigascale DRAM with a Negative Word-Line Scheme", Hitoshi Tanaka et al., IEEE Jurnal of Solid-State Circuits, Vol. 34, No. 8, August 1999, pp. 1084-1090
pl	"A 130-nm 6-GHz 256 x 32 bit Leakage-Tolerant Register File, Ram K. Krishnamurthy, et al., IEEE Journal of Solid-State Circuits, Vol. 37, No. 5, May 2002, pp. 624-632
pl	"Session 10/Low-Power & Communication Signal Processing/Paper FA10.3", Tadahiro Kuroda et al.,
pl	"Dynamic Fine-Grain Leakage Reduction Using Leakage-Biased Bitlines", Seongmoo Heo et al., IEEE Proceedings of the 29th Annual International symposium on Computer Architecture, 2002, 11 pages
pl	"Dynamic Leakage Cut-off Scheme for Low-Voltage SRAM's", Hiroshi Kawaguchi, et al., IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1998, pp. 140-141

Examiner's Signature: Phuong M. Huynh Date Considered: 9/28/05

Initial if reference was considered, whether or not citation is in conformance with MPEP. Mark through citation if not considered. Include a copy of this citation form with your next correspondence to the Applicant(s).